

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

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A

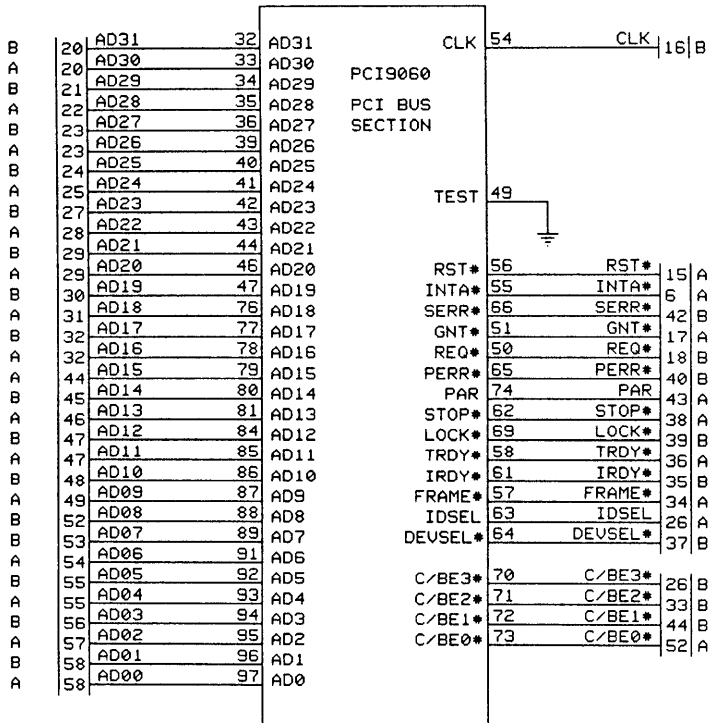
D

C

B

A

A9060
U20A



A | 4 | TDI - TDO boundary scan not supported

B | 11 | PRSNT2* @ GND = 15W max

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PCI BUS I/O

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	10118	REV etch
DATE: 12/05/96 13:38:30		SHEET 01 OF 10

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

SEPARATE 10KOHM PULL-UPS
 NC's SHOULD GO TO VIAS TO NOWHERE!

ALL PINS LABELLED NCxxxx SHOULD
 GO TO VIAS FOR POSSIBLE FUTURE CONNECTION

B9060
 U20B

17 S2 PCI9060
 18 S1 PROCESSOR
 19 S0 INDEPENDENT
 9 MODE1 AND EEPROM
 10 MODE0 SECTION
 20 ADMODE

169 BREQ
 21 BREQ0
 28 BTERM0*
 8 DMPAF*
 165 LDSHOLD
 150 LRESETI*
 23 LSERR*

DON'T WAIT FOR LOCAL SET-UP
 WE COUNT ON ONE WAIT STATE

26 NB*
 149 WAIT0*
 6 WAIT1*

31 USER1
 27 USER0

INTERRUPT FROM FPGA

151 LINTI*
 152 LINTO*

NO LOCAL PARITY

12 DP3
 13 DP2
 14 DP1
 15 DP0
 16 PCHK*

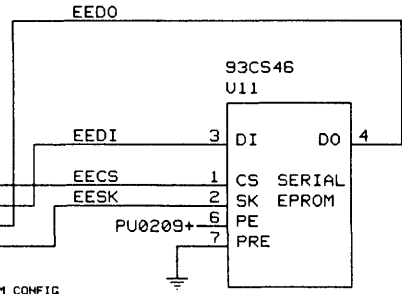
DMA REQ FROM FPGA
 DRIVE BOTH DREQ# SO EITHER
 CHANNEL CAN BE USED

24 DREQ1*
 29 DREQ0*
 25 DACK1*
 30 DACK0*

CLKSEL 170 - PU0210+
 EE1MC 175 - PU0211+
 EECS 176
 EEDI 172
 EEDO 171
 EESK 173
 SHORT* 174 - PU0208+

FOR THE PLX 9080, CLKSEL BECOMES PCIVOLT
 AND EE1MC BECOMES EESL
 KEEP SEPARATE PULL-UPS IN CASE WE
 HAVE TO MOD THESE PINS LATER

USE FULL EEPROM CONFIG
 keep separate pull-up
 for short*. it may need to
 be changed for different eeprom



EEPROM MAY LOAD EXTRA WORDS INTO DIAG REG
 WHICH COULD DISABLE DMA CHANS - SEE DOCS

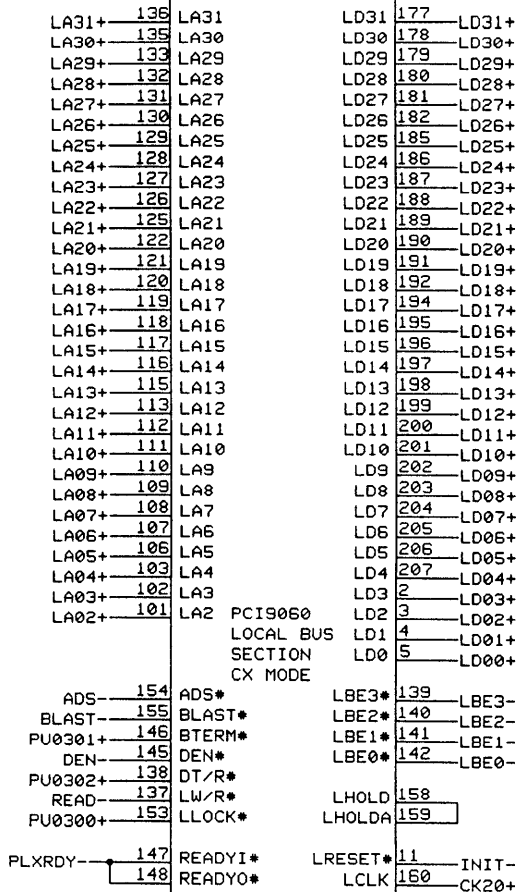
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PROC. IND. LOCAL BUS & EEPROM

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	10118	REV etch
DATE: 12/05/96 13:38:59	SHEET 02 OF 10	

LA14 -- 31 NOT USED - PULLED UP ONLY
 PULL UP ADS, BLAST, DEN, READ
 & READY IN/OUT

C9060
 U20C



THESE ALSO HAVE OTHER MEANINGS WHEN IN 16 BIT MODE

- LBE3 = BHE-
- LBE2 = NC
- LBE1 = LA01+
- LBE0 = BLE-

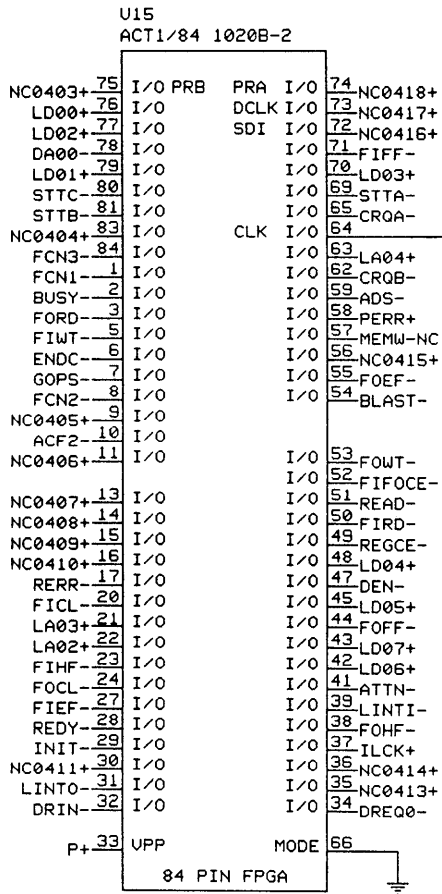
DIRECT SLAVE IO IS 32 BITS
 DMA CHAIN READS AND XFERS ARE 16 BITS

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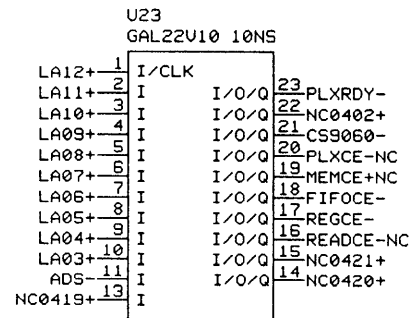
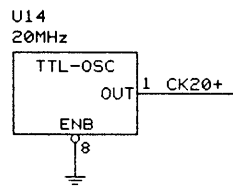
LOCAL BUS

IKON CORPORATION	
PCI DR11 - 1/2 size	
D	10118 REV etch
DATE: 12/05/96 13:39:45	SHEET 03 OF 10

4 DECOUPLERS FOR FPGA



(PLD221)



(PLD222)

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FPGA & GALS

IKON CORPORATION			
PCI DR11 - 1/2 size			
D	10118	REV	etch
DATE: 12/05/96 13:40:32		SHEET 04 OF 10	

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

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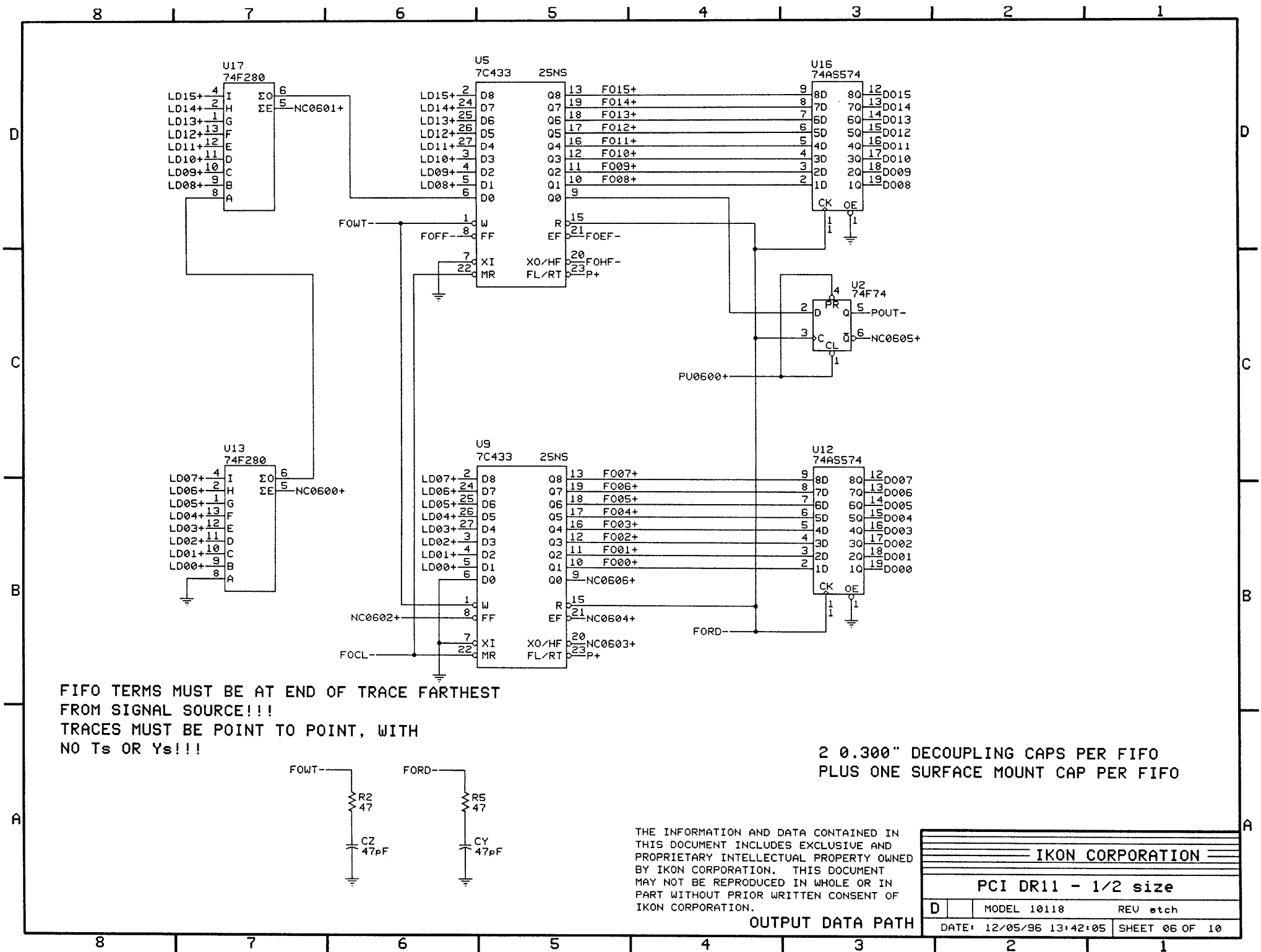
NO LOCAL MEMORY IN 10118

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LOCAL MEMORY

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	10118	REV etch
DATE: 12/05/96 13:41:18		SHEET 05 OF 10

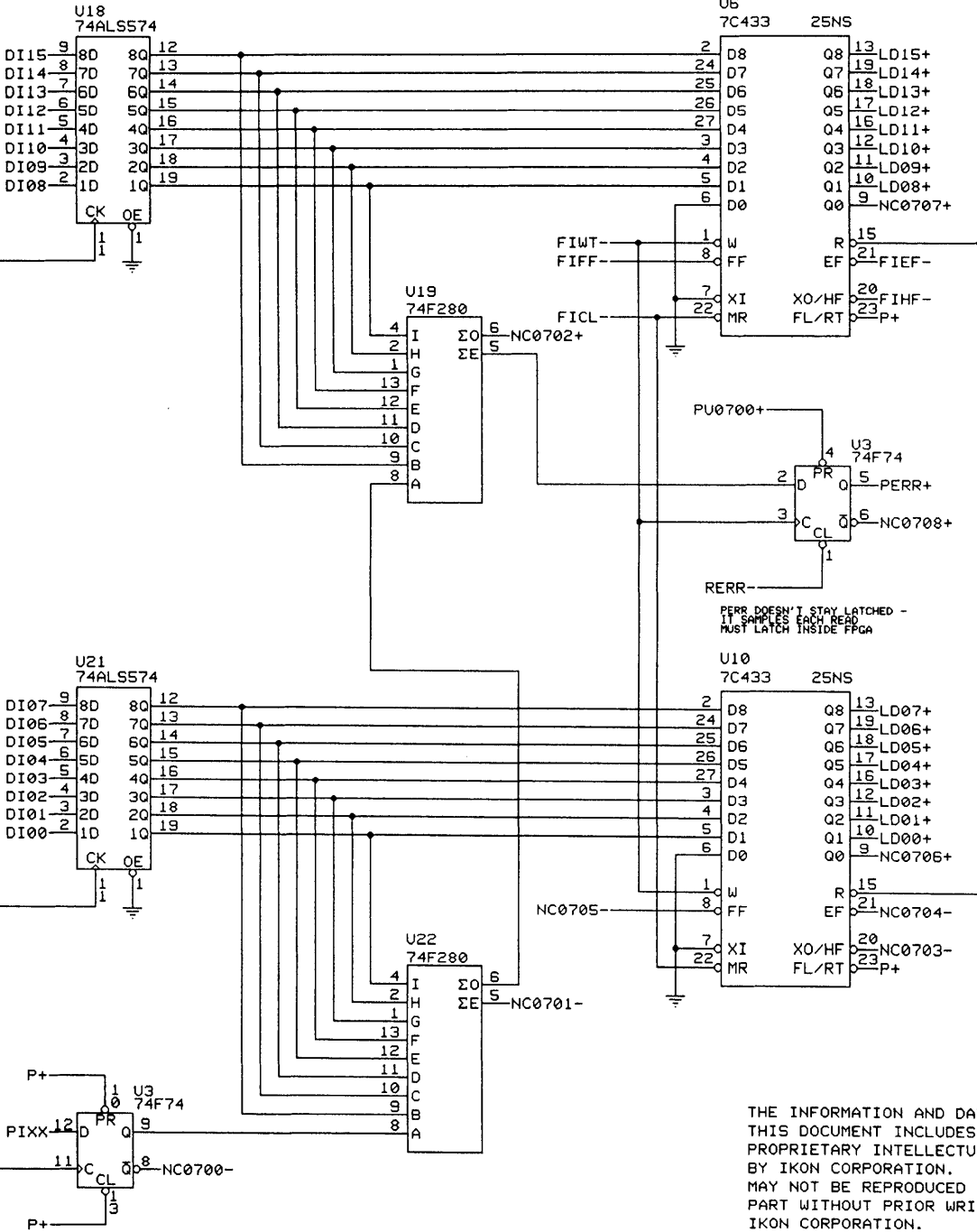
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



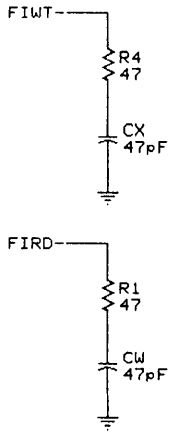
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IKON CORPORATION		
PCI DR11 - 1/2 size		
D	MODEL 10118	REV etch
DATE: 12/05/96 13:42:05	SHEET 06 OF 10	

2 0.300 DECOUPLING CAPS PER FIFO



FIFO TERMS MUST BE AT FAR END OF TRACE FROM SIGNAL SOURCE !!!
 TRACES MUST BE POINT TO POINT, WITH NO Ts OR Ys!!!!

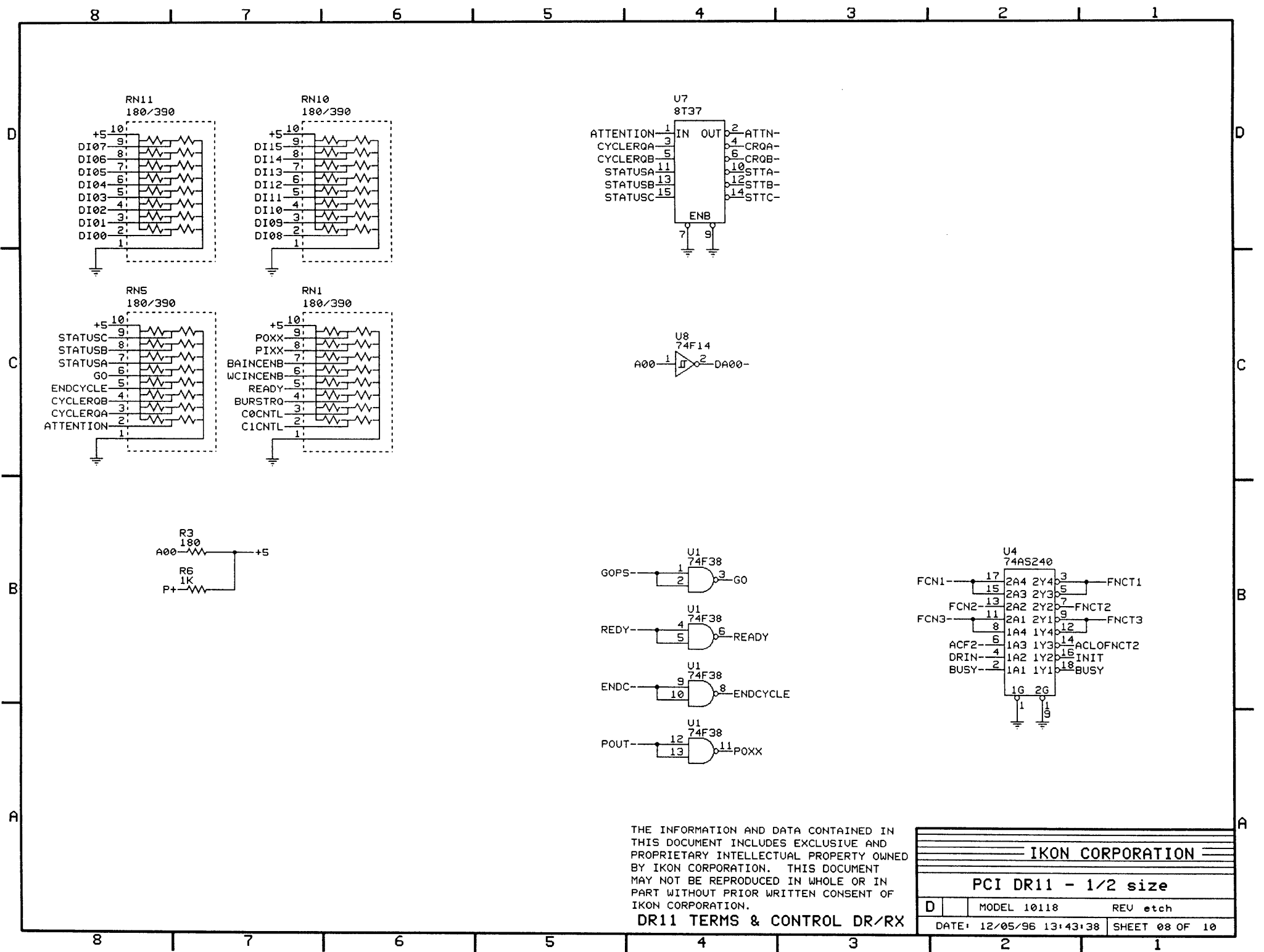


PERR DOESN'T STAY LATCHED - IT SAMPLES EACH READ MUST LATCH INSIDE FPGA

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INPUT DATA PATH

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	MODEL 10118	REV etch
DATE: 12/05/96 13:42:52	SHEET 07 OF 10	



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DR11 TERMS & CONTROL DR/RX

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	MODEL 10118	REV etch
DATE: 12/05/96 13:43:38 SHEET 08 OF 10		

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

D

C

C

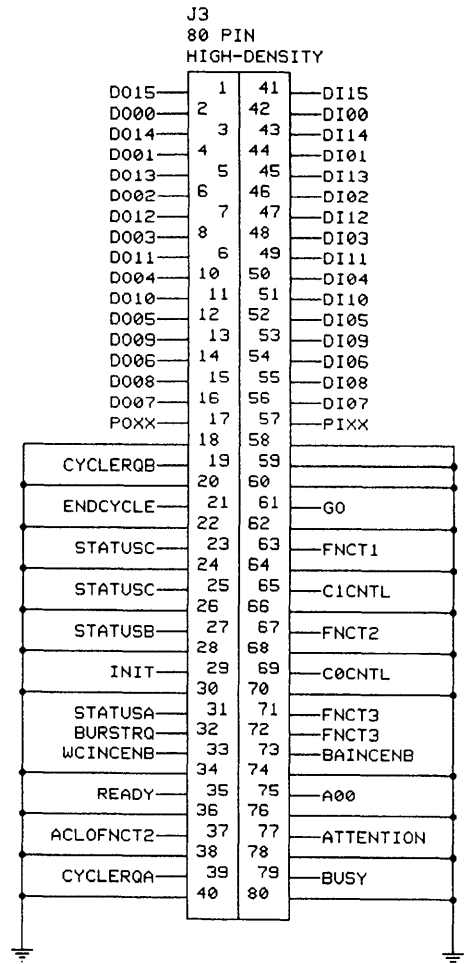
B

B

A

A

NO 40-PIN HEADERS IN 10118

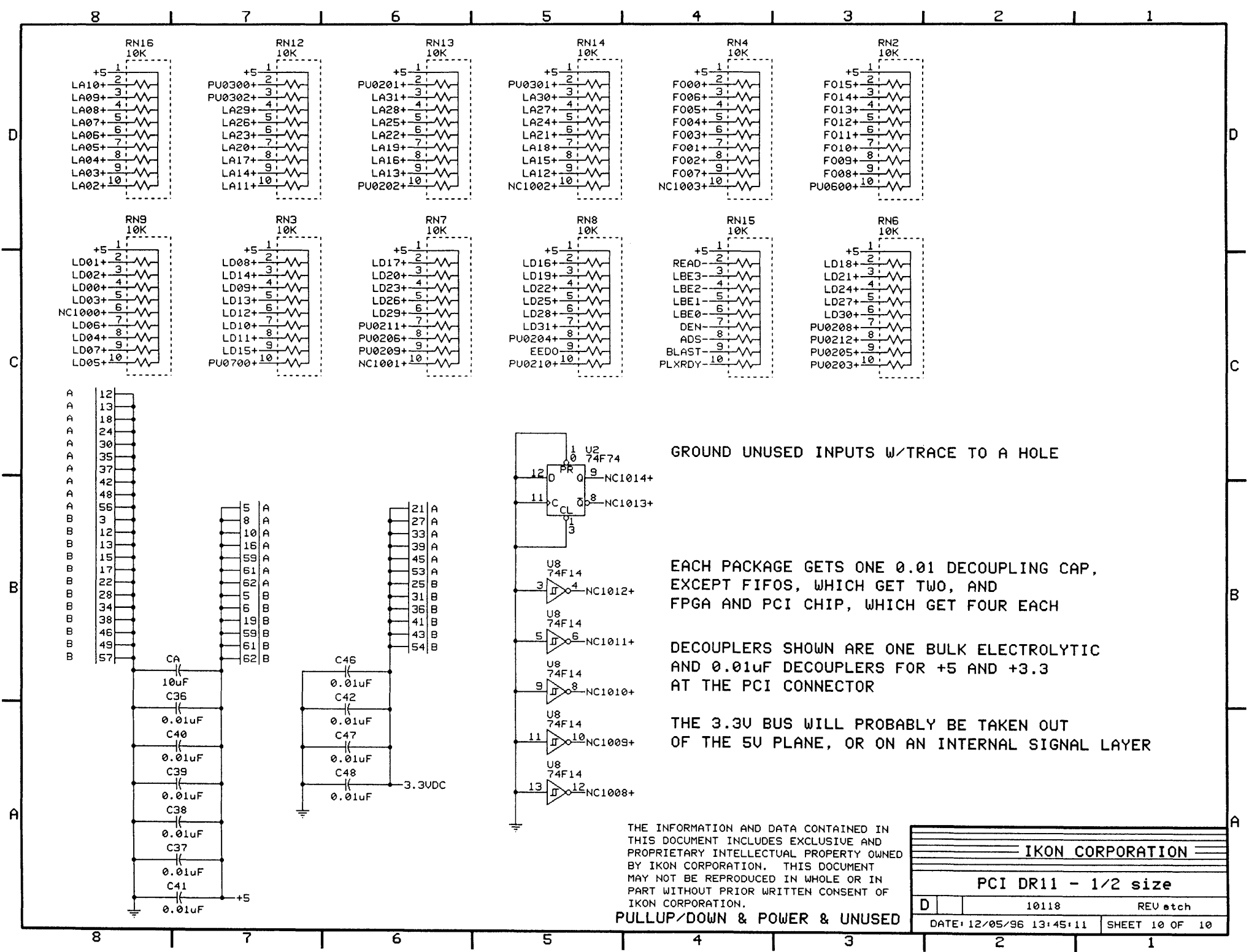


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DR11 CONNECTORS

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	MODEL 10118	REV etch
DATE:	12/05/96 13:44:25	SHEET 09 OF 10

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1



GROUND UNUSED INPUTS W/TRACE TO A HOLE

EACH PACKAGE GETS ONE 0.01 DECOUPLING CAP, EXCEPT FIFOS, WHICH GET TWO, AND FPGA AND PCI CHIP, WHICH GET FOUR EACH

DECOUPLERS SHOWN ARE ONE BULK ELECTROLYTIC AND 0.01uF DECOUPLERS FOR +5 AND +3.3 AT THE PCI CONNECTOR

THE 3.3V BUS WILL PROBABLY BE TAKEN OUT OF THE 5V PLANE, OR ON AN INTERNAL SIGNAL LAYER

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PULLUP/DOWN & POWER & UNUSED

IKON CORPORATION		
PCI DR11 - 1/2 size		
D	10118	REV atch
DATE: 12/05/96 13:45:11		SHEET 10 OF 10