

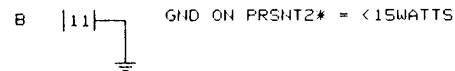
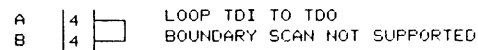
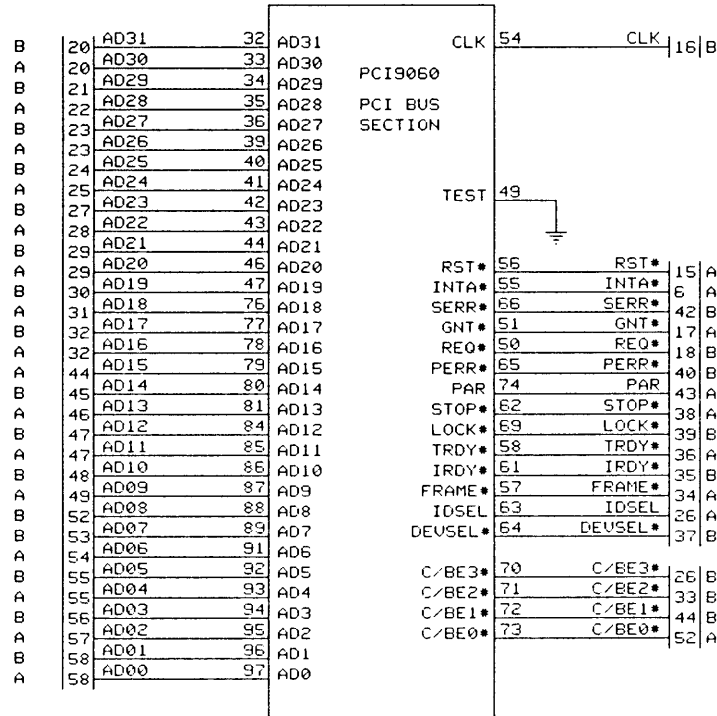
D

C

B

A

A9060
U21A



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PCI BUS I/O

IKON CORPORATION			
PCI Hardcopy (short)			
D	10117	REV	etch
DATE: 02/14/96 10:42:49		SHEET 01 OF 10	

SEPARATE 10KOHM PULL-UPS
 NC's SHOULD GO TO VIAS TO NOWHERE!

B9060
 U21B *U21B*

D

C

B

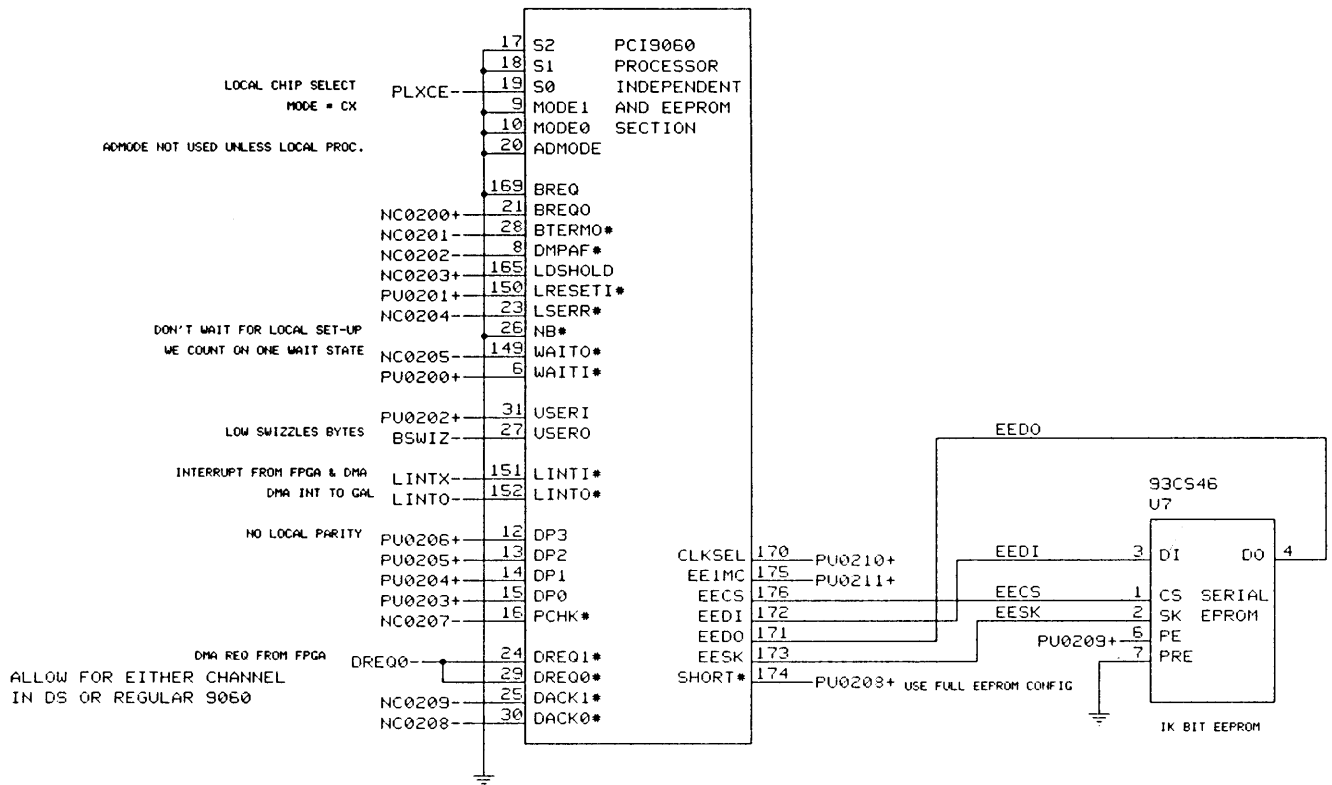
A

D

C

B

A



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IKON CORPORATION		
PCI Hardcopy (short)		
D	10117	REVetch
DATE: 02/14/96 10:43:18		SHEET 02 OF 10

LA13 -- 31 NOT USED - PULLED UP ONLY
 PULL UP ADS, BLAST, DEN, READ

C9060
 U21C *U21C*

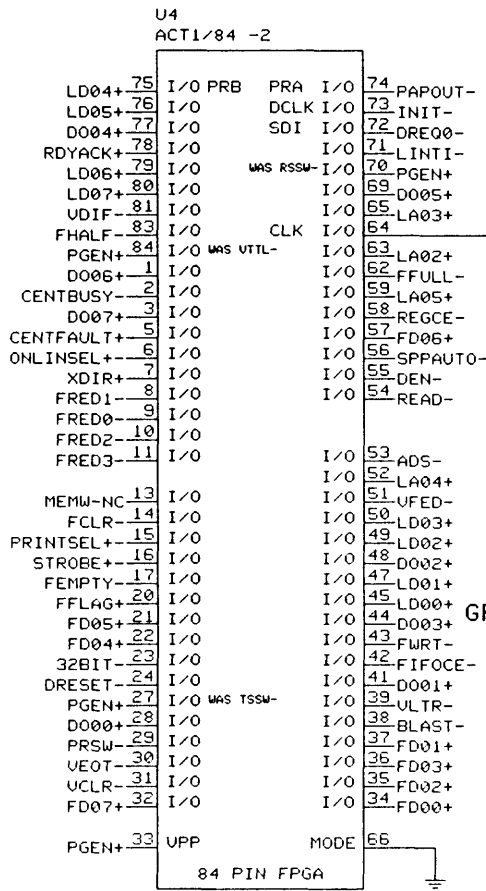
LA31+	136	LA31	LD31	177	LD31+
LA30+	135	LA30	LD30	178	LD30+
LA29+	133	LA29	LD29	179	LD29+
LA28+	132	LA28	LD28	180	LD28+
LA27+	131	LA27	LD27	181	LD27+
LA26+	130	LA26	LD26	182	LD26+
LA25+	129	LA25	LD25	185	LD25+
LA24+	128	LA24	LD24	186	LD24+
LA23+	127	LA23	LD23	187	LD23+
LA22+	126	LA22	LD22	188	LD22+
LA21+	125	LA21	LD21	189	LD21+
LA20+	122	LA20	LD20	190	LD20+
LA19+	121	LA19	LD19	191	LD19+
LA18+	120	LA18	LD18	192	LD18+
LA17+	119	LA17	LD17	194	LD17+
LA16+	118	LA16	LD16	195	LD16+
LA15+	117	LA15	LD15	196	LD15+
LA14+	116	LA14	LD14	197	LD14+
LA13+	115	LA13	LD13	198	LD13+
LA12+	113	LA12	LD12	199	LD12+
LA11+	112	LA11	LD11	200	LD11+
LA10+	111	LA10	LD10	201	LD10+
LA09+	110	LA9	LD9	202	LD09+
LA08+	109	LA8	LD8	203	LD08+
LA07+	108	LA7	LD7	204	LD07+
LA06+	107	LA6	LD6	205	LD06+
LA05+	106	LA5	LD5	206	LD05+
LA04+	103	LA4	LD4	207	LD04+
LA03+	102	LA3	LD3	2	LD03+
LA02+	101	LA2	LD2	3	LD02+
		PCI9060	LD1	4	LD01+
		LOCAL BUS SECTION	LD0	5	LD00+
		CX MODE			
ADS-	154	ADS*	LBE3*	139	LBE3-
BLAST-	155	BLAST*	LBE2*	140	LBE2-
PU0301+	146	BTERM*	LBE1*	141	LBE1-
DEN-	145	DEN*	LBE0*	142	LBE0-
PU0302+	138	DT/R*			
READ-	137	LW/R*	LHOLD	158	
PU0300+	153	LLOCK*	LHOLDA	159	
PLXRDY-	147	READYI*	LRESET*	11	INIT-
	148	READYO*	LCLK	150	CK20+

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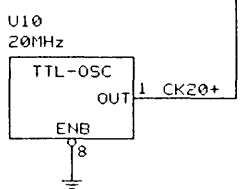
LOCAL BUS

IKON CORPORATION			
PCI Hardcopy (short)			
D	10117	REV	etch
DATE: 02/14/96 10:44:04		SHEET 03 OF 10	

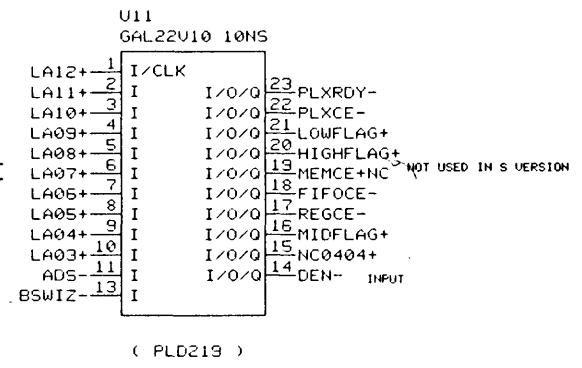
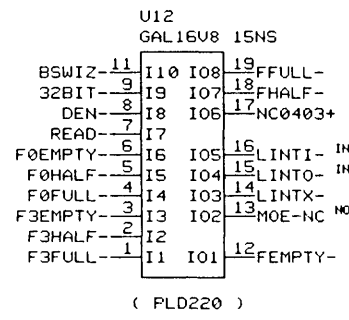
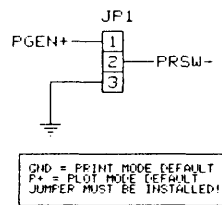
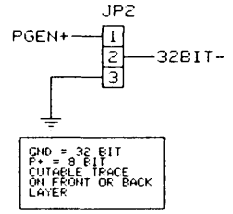
4 DECOUPLERS FOR FPGA



(PLD218)



GROUND 32BIT- WITH CUTABLE TRACE



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FPGA & GALS

IKON CORPORATION			
PCI Hardcopy (short)			
D	10117	REV	etch
DATE: 02/14/96 10:44:51		SHEET 04 OF 10	

8 7 6 5 4 3 2 1

D
C
B
A

D
C
B
A

NO LOCAL MEMORY IN S VERSION

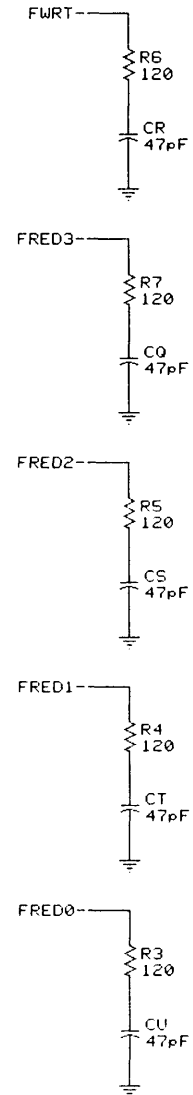
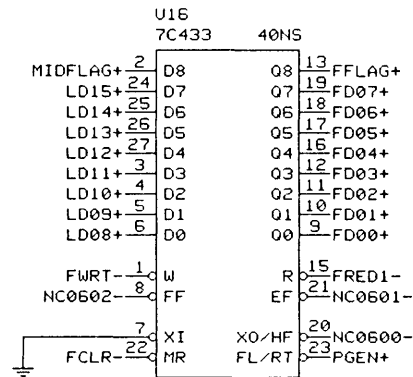
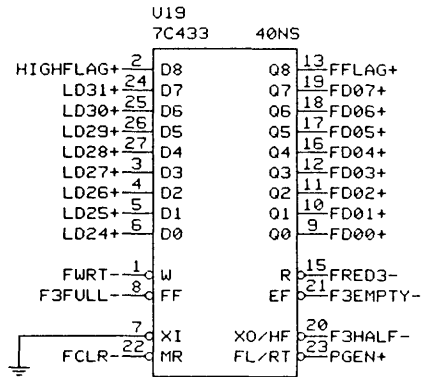
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LOCAL MEMORY

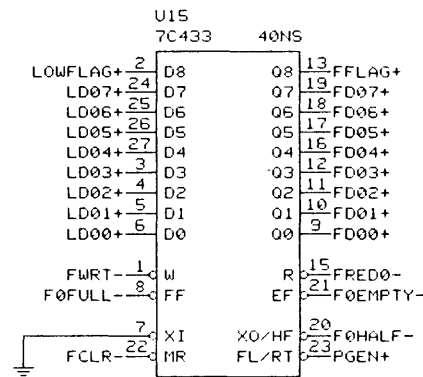
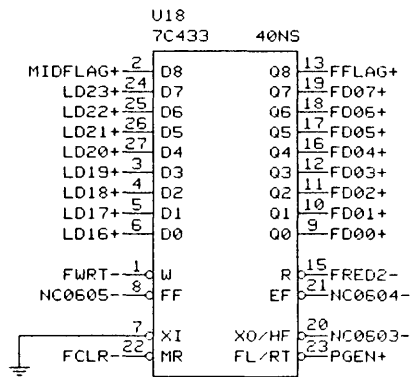
IKON CORPORATION		
PCI Hardcopy (short)		
D	10117	REV etch
DATE: 02/14/96 10:45:37		SHEET 05 OF 10

8 7 6 5 4 3 2 1

TERMINATIONS AT FIFO END OF EACH R/W RUN!
NO Ts OR Ys (SOURCE END IS FPGA)



FIFOS SHARE A PULLUP



TWO DECOUPLERS PER FIFO

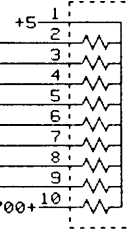
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FIFOS

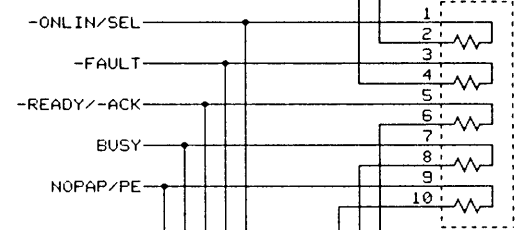
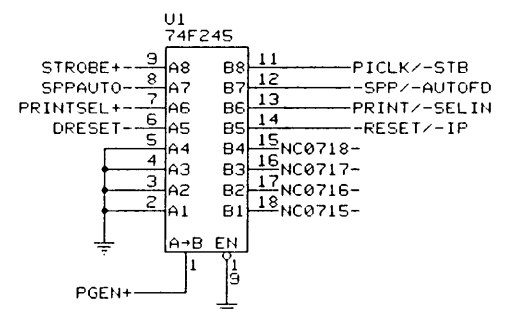
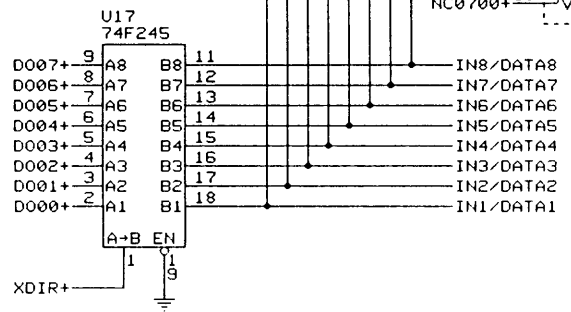
IKON CORPORATION		
PCI Hardcopy (short)		
D	10117	REV etch
DATE: 02/14/96 10:46:24	SHEET 06 OF 10	

THIS NET TO BE USED FOR OUTPUT BITS ONLY

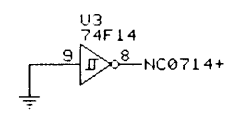
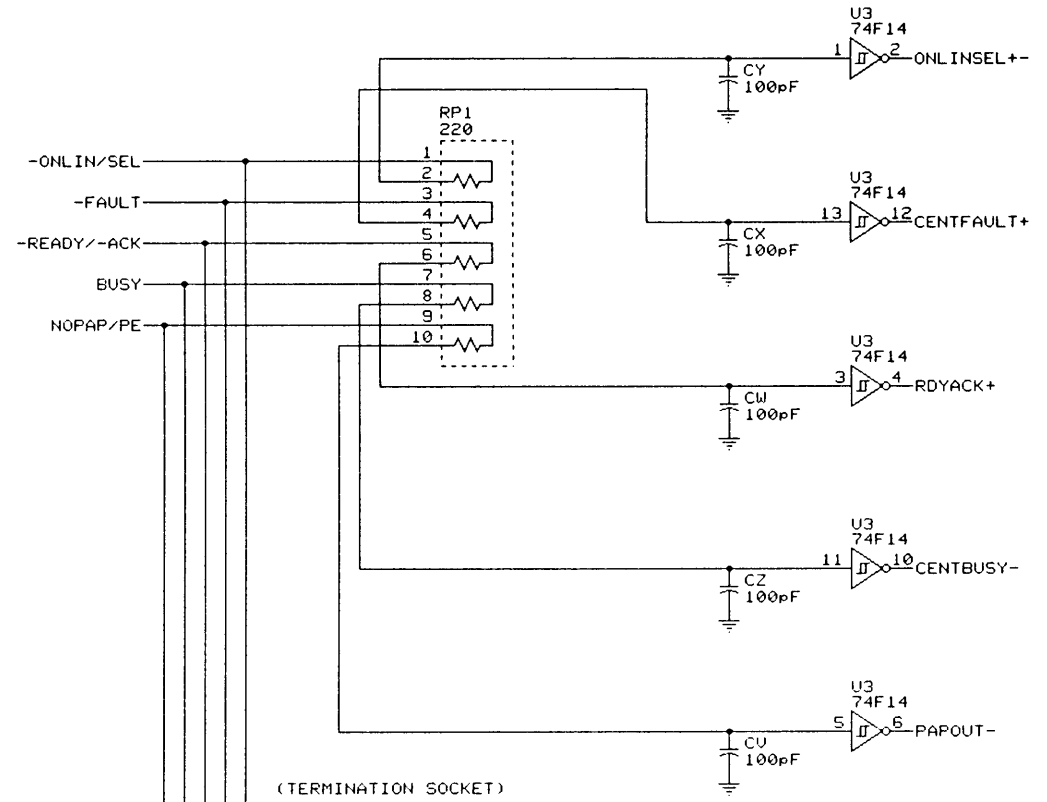
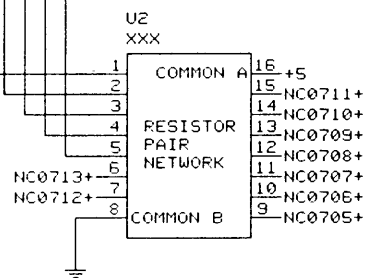
RP14
470



NC0700+



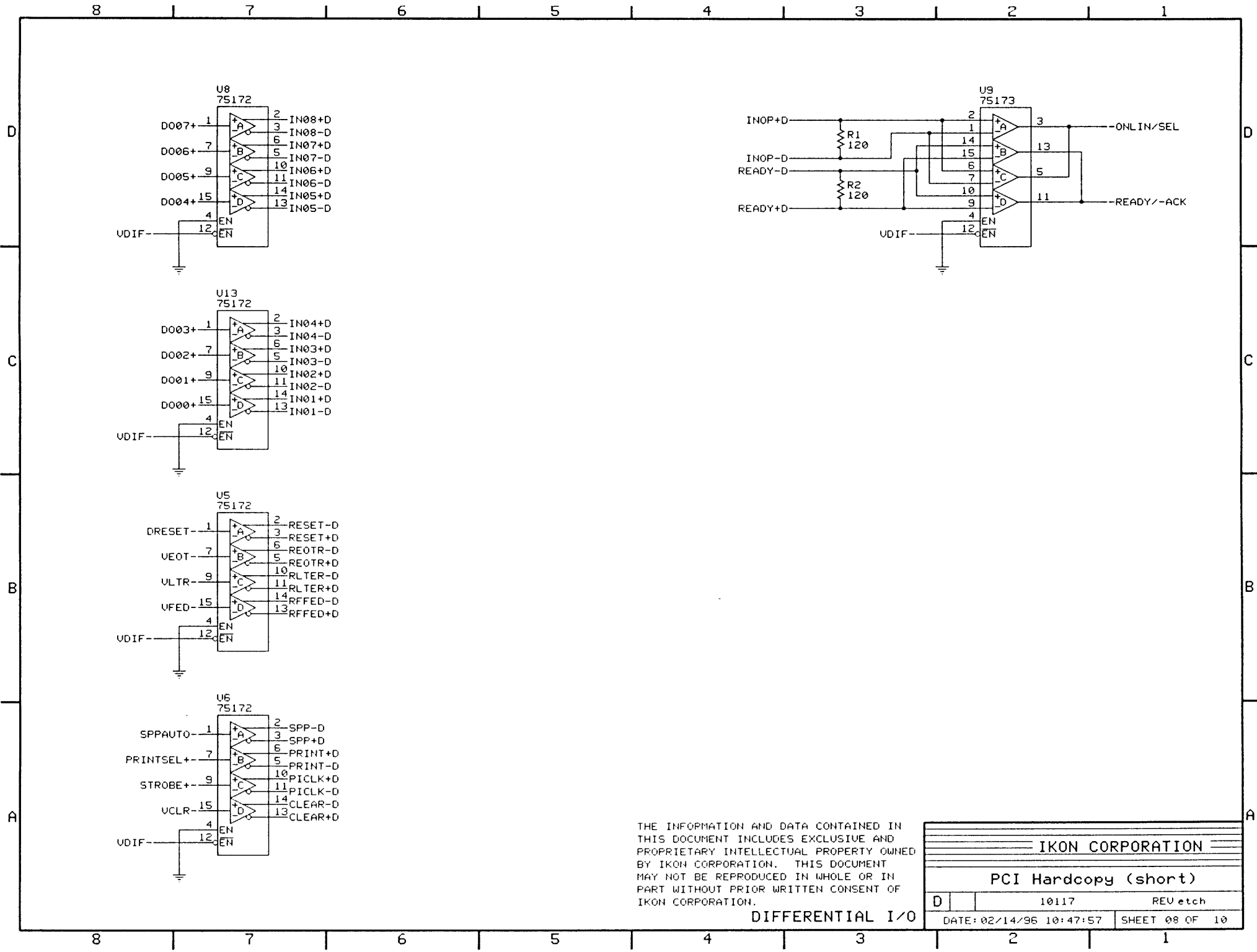
(TERMINATION SOCKET)



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TTL I/O

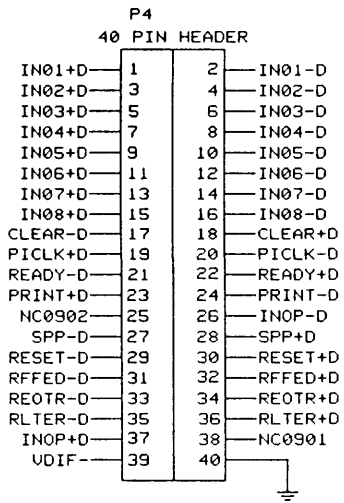
IKON CORPORATION		
PCI Hardcopy (short)		
D	10117	REV etch
DATE: 02/14/96 10:47:10	SHEET 07 OF 10	



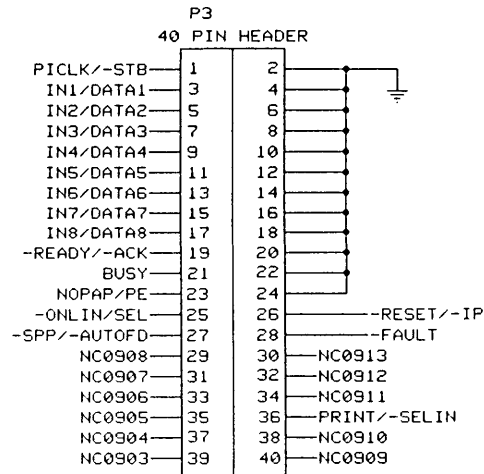
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DIFFERENTIAL I/O

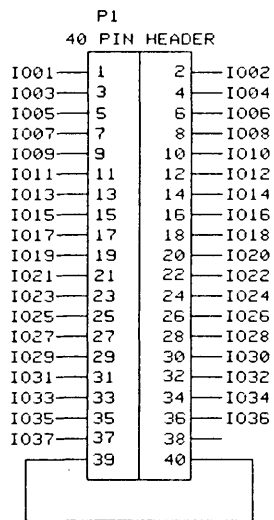
IKON CORPORATION		
PCI Hardcopy (short)		
D	10117	REV etch
DATE: 02/14/96 10:47:57		SHEET 08 OF 10



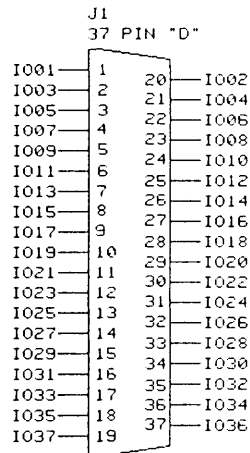
(VERSATEC DIFFERENTIAL)



(CENTRONICS)



(I/O CONNECTOR)



(TO DEVICE)

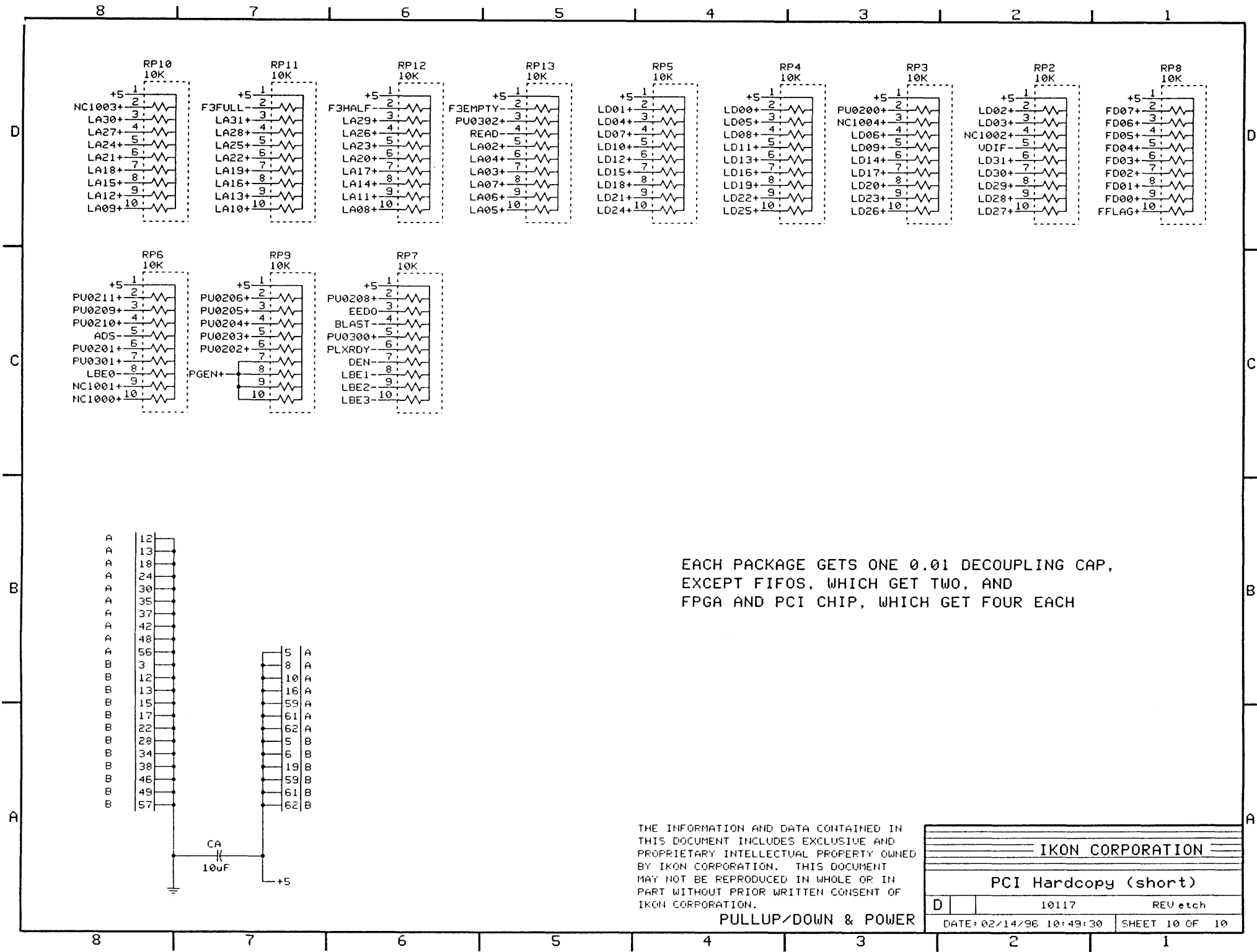
INTERNAL JUMPER CABLE IS CONNECTED
BETWEEN P4 AND ONE OF P1, 2, OR 3

P4 AND J1 ARE CONNECTED PIN-FOR-PIN
BY MECHANICAL CORRESPONDENCE,
NOT PIN NUMBER

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I/O CONNECTORS

IKON CORPORATION			
PCI Hardcopy (short)			
D	10117	REV etch	
DATE: 02/14/96 10:48:44		SHEET 09 OF 10	



EACH PACKAGE GETS ONE 0.01 DECOUPLING CAP,
EXCEPT FIFOS, WHICH GET TWO, AND
FPGA AND PCI CHIP, WHICH GET FOUR EACH

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PULLUP/DOWN & POWER

IKON CORPORATION		
PCI Hardcopy (short)		
D	10117	REU etch
DATE: 02/14/96 10:49:30		SHEET 10 OF 10